WHAT IS CLAIMED IS:

1. A method of generating test patterns, comprising the steps of:

providing a test pattern suitable for testing a test circuit;

listing out and analyzing the test pattern;

converting the test pattern into a digital circuit description language program and simulating the digital circuit description language program to produce a simulated test pattern, applying the simulated test pattern on the test circuit to obtain simulated test results;

writing the digital circuit description language program into a memory unit;

testing the test circuit using the program inside the memory unit to produce actual test results; and

comparing the simulated test results with the actual test results:

if the simulated results and the actual results match each other, the test circuit is repeatedly tested using the program inside the memory unit until no delay is found between loop backs; and

if there is a mismatch between the simulated results and the actual results, the digital circuit description language program is adjusted and written back to the memory unit anew.

2. The test pattern generation method of claim 1, wherein the digital circuit description language includes a VHDL language.

3. The test pattern generation method of claim 1, wherein the memory unit includes a field programmable gate array.

4. The test pattern generation method of claim 2, wherein the digital circuit

description language program further includes test pattern data program codes and test pattern length program codes.

5. The test pattern generation method of claim 4, wherein the step of using the digital circuit description language program inside the memory unit to test the test circuit includes the following sub-steps:

resetting a counter;

initializing a counting procedure according to a test pattern cycle and testing the test circuit with test data signals and test length signals generated by the test pattern data program code and the test pattern length program code according to the count;

the test circuit producing test result signals at the end of the testing operation; and

comparing the test result signals with normal test result signals:

if the test signals and the normal signals match each other, a normal indicator signal is issued; and

if there is a mismatch between the test signals and the normal signals, an error indicator signal is issued.

6. A test pattern generator for testing a test circuit, comprising:

a first read-only-memory unit, wherein the first read-only-memory unit holds test pattern data program codes and outputs test data signals;

a second read-only-memory unit, wherein the second read-only-memory unit holds test pattern length codes and outputs test length signals;

a counter electrically coupled to the first read-only-memory unit and the second read-only-memory unit, wherein the counter counts according to a test pattern

cycle;

a test circuit connector electrically coupled to the first read-only-memory unit and the second read-only-memory unit, wherein the test circuit connector outputs test result signals;

a comparator, wherein the comparator holds a normal test result waveform, couples electrically with the test circuit, the first read-only-memory unit and the second read-only-memory unit and outputs an indicator signal; and

a control device electrically coupled to the first read-only-memory unit, the second read-only-memory unit, the counter and the comparator, wherein the control device receives a control signal and outputs the indicator signal.

7. The test pattern generator of claim 6, wherein the counter includes a decrement counter.

8. The test pattern generator of claim 6, wherein the counter includes a system containing a decrement counter and an increment counter.

9. The test pattern generator of claim 6, wherein the comparator further includes a built-in third read-only-memory unit for holding normal test result signals.

10. The pattern generator of claim 6, wherein the first read-only-memory unit, the second read-only-memory unit, the counter, the comparator and the control device may be implemented using a single field programmable gate array.

11. A test pattern generator for generating a test pattern to test a test circuit, comprising:

a switching device for outputting a control signal;

a field programmable gate array for receiving the control signal and test result signals and outputting test data signals, test length signals and an indicator signal;

a test circuit connector for receiving the test data signals and the test length signals and outputting the test result signals;

an output buffer for receiving the indicator signal and outputting an output signal;

a display device for receiving the output signal; and

an interface device electrically coupled with the switching device, the field programmable gate array, the test circuit connector, the output buffer and the display device.

12. The test pattern generator of claim 11, wherein the switching device includes a 3-bit finger switch.

13. The test pattern generator of claim 11, wherein the field programmable gate array may further include the following sub-components:

a first read-only-memory unit, wherein the first read-only-memory unit holds test pattern data program codes and outputs test data signals;

a second read-only-memory unit, wherein the second read-only-memory unit holds test pattern length codes and outputs test length signals;

a counter electrically coupled to the first read-only-memory unit and the second read-only-memory unit, wherein the counter counts according to a test pattern cycle;

a comparator, wherein the comparator holds a normal test result waveform, couples electrically with the test circuit, the first read-only-memory unit and the second read-only-memory unit and outputs the indicator signal; and

a control device electrically coupled to the first read-only-memory unit, the second read-only-memory unit, the counter and the comparator, wherein the control

device receives a control signal and outputs the indicator signal.

14 ~~13~~. The test pattern generator of claim 11, wherein the output buffer includes a plurality of 74LS244 integrated circuits.

15 ~~14~~. The test pattern generator of claim 11, wherein the display device includes a light-emitting diode display panel.

16 ~~15~~. The test pattern generator of claim 11, wherein the interface device includes an interface board having 128 leads altogether.

17 ~~16~~. The test pattern generator of claim 13, wherein the counter includes a decrement counter.

18 ~~17~~. The test pattern generator of claim 13, wherein the counter includes a system containing a decrement counter and an increment counter.

19 ~~18~~. The test pattern generator of claim 13, wherein the comparator further includes a built-in third read-only-memory unit for holding normal test result signals.